

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE


[Membership](#) [Publications/Services](#) [Standards](#) [Conferences](#) [Careers/Jobs](#)
IEEE Xplore®
 RELEASE 1.8

 Welcome
 United States Patent and Trademark Office


» Search

[Help](#) [FAQ](#) [Terms](#) [IEEE Peer Review](#)
[Quick Links](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced
- ☐ CrossRef

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE Enterprise

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

Your search matched **7** of **1085387** documents.A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.**Refine This Search:**

You may refine your search by editing the current search expression or entering new one in the text box.

current mirror amplifier

Search

☐ Check to search within this result set**Results Key:****JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard**1 Adjustable bidirectional MOS current mirror/amplifier**

Wang, Z.; Guggenbuhl, W.;

Electronics Letters, Volume: 25, Issue: 10, 11 May 1989
Pages: 673 - 675
[\[Abstract\]](#) [\[PDF Full-Text \(204 KB\)\]](#) **IEEE JNL**
2 A CMOS current-mirror amplifier with compact slew rate enhancement circuit for large capacitive load applications

Hoi Lee; Mok, P.K.T.;

Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on, Volume: 1, 6-9 May 2001
Pages: 220 - 223 vol. 1
[\[Abstract\]](#) [\[PDF Full-Text \(332 KB\)\]](#) **IEEE CNF**
3 Fully balanced CMOS current-mode circuits

Zele, R.H.; Allstot, D.J.; Fiez, T.S.;

Solid-State Circuits, IEEE Journal of, Volume: 28, Issue: 5, May 1993
Pages: 569 - 575
[\[Abstract\]](#) [\[PDF Full-Text \(716 KB\)\]](#) **IEEE JNL**
4 A 17-ns 4-Mb CMOS DRAM

Nagai, T.; Numata, K.; Ogihara, M.; Shimizu, M.; Imai, K.; Hara, T.; Yoshida, Saito, Y.; Asao, Y.; Sawada, S.; Fujii, S.;

Solid-State Circuits, IEEE Journal of, Volume: 26, Issue: 11, Nov. 1991
Pages: 1538 - 1543
[\[Abstract\]](#) [\[PDF Full-Text \(692 KB\)\]](#) **IEEE JNL**

5 A block-oriented RAM with half-sized DRAM cell and quasi-folded data line architecture*Kimura, K.; Sakata, T.; Itoh, K.; Kaga, T.; Nishida, T.; Kawamoto, Y.;*

Solid-State Circuits, IEEE Journal of , Volume: 26 , Issue: 11 , Nov. 1991

Pages:1511 - 1518

[\[Abstract\]](#) [\[PDF Full-Text \(816 KB\)\]](#) **IEEE JNL**

6 Single-point-detection slew-rate enhancement circuits for single-stage amplifiers*Hoi Lee; Mok, P.K.T.;*

Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on , Volume: 2 , 26-29 May 2002

Pages:II-831 - II-834 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(569 KB\)\]](#) **IEEE CNF**

7 An experimental 1.5-V 64-Mb DRAM*Nakagome, Y.; Tanaka, H.; Takeuchi, K.; Kume, E.; Watanabe, Y.; Kaga, T.; Kawamoto, Y.; Murai, F.; Izawa, R.; Hisamoto, D.; Kisu, T.; Nishida, T.; Takeuchi, E.; Itoh, K.;*

Solid-State Circuits, IEEE Journal of , Volume: 26 , Issue: 4 , April 1991

Pages:465 - 472

[\[Abstract\]](#) [\[PDF Full-Text \(808 KB\)\]](#) **IEEE JNL**

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved